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10/574,290	03/31/2006	Mitsuaki Osame	0756-7670	7471

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,290	OSAME ET AL.	
	Examiner	Art Unit	
	LONG NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 22-28* is/are pending in the application.

4a) Of the above claim(s) *7-18* is/are withdrawn from consideration.

5)☒ Claim(s) *22-24* is/are allowed.

6)☒ Claim(s) *1-6 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al. (USP 5,198,699).

With respect to claims 1, 2 and 25, Figure 4 of Hashimoto et al. discloses a semiconductor device, which includes: a first transistor (P-channel transistor 92), a second transistor (N-channel transistor 94), a third transistor (P-channel transistor 96), a first power source (100) applying a first potential (power supply such as Vdd), a second power source (ground) applying a second potential (ground); and a circuit (130, 134) for applying a third potential (Vy) which is different from the first potential and the second potential; a first signal (signal at node 38), a second signal (signal at node 34) with the connections as recited in the claims. Note that it is old and well known in the art that a transistor, when turning on, forms a resistor, and during the operation of the circuitry in Figure 4 of Hashimoto et al., the transistors 114 and 116 in the voltage divider circuit (114, 116), and the transistors 130 and 114 in the voltage divider (130, 134) are ON, so each of the transistors 114, 116, 130 and 134 forms a resistor. Thus, the circuit (114, 116) and the circuit (130, 134) each includes multiple resistors connected in series between the first power source (supply Vdd of the circuit) and the second

power source (ground) and a potential is outputted from the connecting node of two resistors of each circuit.

With respect to claims 3 and 4, Figure 4 of Hashimoto et al. discloses a semiconductor device, which includes: a first transistor (P-channel transistor 92), a second transistor (N-channel transistor 94), a third transistor (N-channel transistor 90), a first power source (100) applying a first potential (power supply such as Vdd), a second power source (ground) applying a second potential (ground); and a circuit (114, 116) for generating a third potential (Vx) which is different from the first potential and the second potential; a first signal (signal at node 38), a second signal (signal at node 34) with the connections as recited in the claims. Note that it is old and well known in the art that a transistor, when turning on, forms a resistor, and during the operation of the circuitry in Figure 4 of Hashimoto et al., the transistors 114 and 116 in the voltage divider circuit (114, 116), and the transistors 130 and 114 in the voltage divider (130, 134) are ON, so each of the transistors 114, 116, 130 and 134 forms a resistor. Thus, the circuit (114, 116) and the circuit (130, 134) each includes multiple resistors connected in series between the first power source (supply Vdd of the circuit) and the second power source (ground) and a potential is outputted from the connecting node of two resistors of each circuit.

With respect to claims 5 and 6, Figure 4 of Hashimoto et al. discloses a semiconductor device, which includes: a first transistor (P-channel transistor 92), a second transistor (N-channel transistor 94), a third transistor (P-channel transistor 96), a fourth transistor (N-channel transistor 90), a first power source (100) applying a first potential (power supply such as Vdd), a second power source (ground) applying a second potential (ground), a first circuit (130, 134) for applying a third potential (Vy) which is different from the first potential and the second potential,

a second circuit (114, 116) for generating a fourth potential (Vx) which is different form the first potential and the second potential, a first signal (signal at node 38), a second signal (signal at node 34) with the connections as recited in the claims. Note that it is old and well known in the art that a transistor, when turning on, forms a resistor, and during the operation of the circuitry in Figure 4 of Hashimoto et al., the transistors 114 and 116 in the voltage divider circuit (114, 116), and the transistors 130 and 114 in the voltage divider (130, 134) are ON, so each of the transistors 114, 116, 130 and 134 forms a resistor. Thus, the circuit (114, 116) and the circuit (130, 134) each includes multiple resistors connected in series between the first power source (supply Vdd of the circuit) and the second power source (ground) and a potential is outputted from the connecting node of two resistors of each circuit.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. (USP 5,198,699) in view of Uchiki et al. (USP 6,646,486).

With respect to claim 26-28, Figure 4 of Hashimoto et al. teaches all the limitations of these claims as discussed in the 102 rejection above except for each of the multiple resistors has a resistance which is constant regardless of a voltage applied thereto. However, Figure 12C of the Uchiki et al. teaches a voltage divider generator circuit that includes a plurality of resistors wherein each of the multiple resistors has a resistance which is constant regardless of a voltage

applied thereto. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuitry of Hashimoto et al. by replacing each of the voltage divider 114-116 and 130-134 with the specific voltage divider having fix resistance value as taught in Figure 12C of Uchiki et al. for the purpose of easily achieving a known reference voltage based on the ratio of the fixed resistances of the resistors. Thus, this modification/combination meets all the limitations of claims 26-28.

Allowable Subject Matter

5. Claims 22-24 are presently allowed.

Response to Arguments

6. Applicant's arguments filed on 4/6/09 have been fully considered but they are not persuasive.

Applicant argues that Hashimoto does not teaches multiple resistors connected in series, that is, each of the resistors have a fixed resistance. However, this argument is not persuasive because the limitation that each resistor has a fixed resistance is not recited in the claim. Further, for broadest reasonable interpretation, it is old and well known in the art that a transistor, when turning on, forms a resistor, and during the operation of the circuitry in Figure 4 of Hashimoto et al., the transistors 114 and 116 in the voltage divider circuit (114, 116), and the transistors 130 and 114 in the voltage divider (130, 134) are ON, so each of the transistors 114, 116, 130 and 134 forms a resistor. Thus, the circuit (114, 116) and the circuit (130, 134) each includes multiple resistors connected in series between the first power source (supply Vdd of the circuit) and the second power source (ground) and a potential is outputted from the connecting node of two resistors of each circuit.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Long Nguyen/
Primary Examiner
Art Unit 2816